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# INTERFACING GUIDE FOR
# iCOM MODEL FD360/CF360
# FLOPPY DISK SYSTEM

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## I. GENERAL

The iCOM Model CF360 Controller/Formatter is designed for use by OEM's in industrial, commerical, and development applications. It is used in the iCOM FD360 series Floppy Disk System as well.

The CF360 can accomodate from one to four floppy disk drives and includes a general purpose interface compatible with most microprocessors and minicomputers.

The CF360 offers many features which reduce computer service overhead. For example, the controller is fully IBM 3740 and 3540 compatible, with all formatting and deformatting accomplished automatically within the controller. The controller also performs track seek/verify, and CRC (Cyclic Redundancy Check) generation and verification automatically.

Independent 128 byte (full-sector) input and output buffers offer the possibility for DMA or programmed I/O operation. The ability to write-protect individual drives also is provided by the controller.

Interface signals to the CPU/MPU are TTL compatible and consist of independent input and output parallel data lines and an 8 bit parallel control port. Upon command, controller status data is presented to the CPU via the input data lines.

## II. PHYSICAL DESCRIPTION

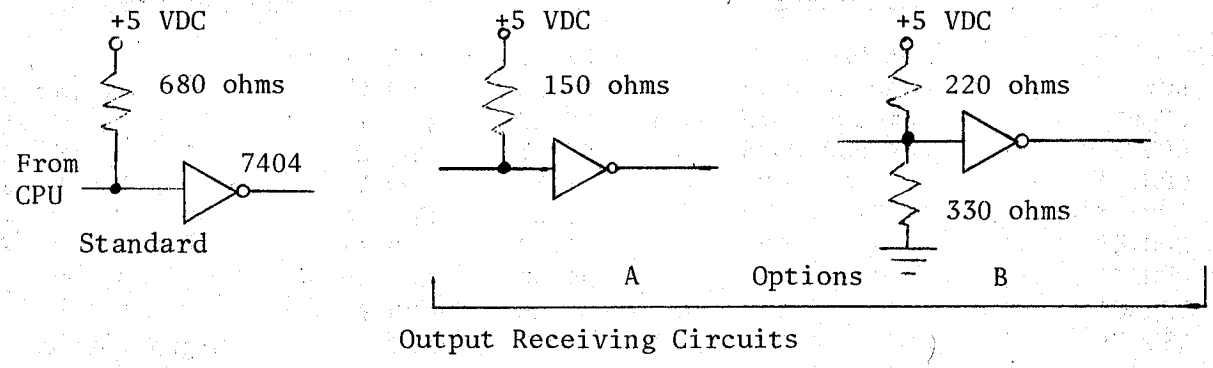
The CF360 is housed on two 7.25 X 15 inch (18.4 X 38.1 cm) printed circuit boards containing a total of about 125 IC's.

Interface connections are provided along one long edge of each board, obviating the need for back-plane wiring or a card cage.

## III. ELECTRICAL INTERFACE

3.1 Signal Levels - All signals are standard TTL-compatible negative true. Positive true all ports available as an option.

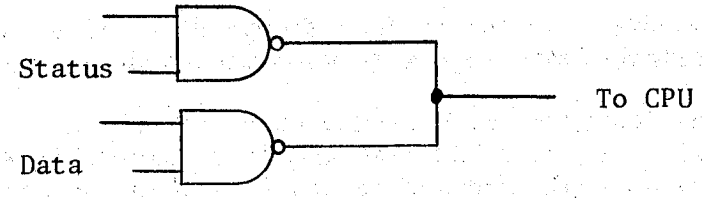
3.1.1 Output to FD360 (negative true)
Logic "0": 2.0V min to +5V max
Logic "1": 0.0V min to 0.8V max
Standard load is 1 TTL Gate (7404 plus 680 ohms to +5V (see Fig. 1). The two other input load variations as shown in Fig. 1 are available as options.




Output Receiving Circuits

Fig. 1

3.1.2 Input from FD360 (negative true)
Logic "0": 2.4V min
Logic "1": 0.0V min to 0.4V max
Current sink at logic "1" is 32 ma (See Fig. 2)




DM 8096 (Tri-State)

Input Status/Data Drive Circuits

Fig. 2

3.2 Pin Configuration - Two 40 conductor 3M-type ribbon cables with socket connectors on each end are normally used for interfacing the CF360. Connectors which mate with the CF360 are 3M #3432-2002 (solder tail) or 3432-4005 (wire wrap posts).

3.3.1 P4 Input Connector (to CPU)

| PIN# | SIGNAL NAME | DESCRIPTION |
|---|---|---|
| P4 1-27 | - | Not used |
| P4 28 | Key or Done | Connector Key<br>Operation Done (option) |
| P4 29 | DI Ø | Data In Ø (LSB)/Busy |
| P4 30 | DI 1 | Data In 1/ UNØ |
| P4 31 | DI 2 | Data In 2/ UN1 — Unit Select |
| P4 32 | DI 3 | Data In 3/ CRC Error |
| P4 33 | DI 4 | Data In 4/ Write Portected |
| P4 34 | DI 5 | Data In 5/ Drive Fail |
| P4 35 | DI 6 | Data In 6/ Not Used |
| P4 36 | DI 7 | Data In 7/ Deleted Data Address Mark |
| P4 37-40 | GRD | Signal Ground |

3.2.2 P5 Output Connector (from) CPU)

| PIN# | SIGNAL NAME | DESCRIPTION | PIN# | SIGNAL NAME | DESCIRPTION |
|---|---|---|---|---|---|
| P5 1-18 | - | Not Used | P5 28 | Not Used | |
| P5 19 | Key | Connector Key | P5 29 | CDO Ø* | Data out Bit Ø |
| P5 20 | CPUØ* | Command Word Strobe | P5 30 | CDO 1* | " " " 1 |
| P5 21 | CPU 1* | Command Word | P5 31 | CDO 2* | " " " 2 |
| P5 22 | CPU 2* | " " | P5 32 | CDO 3* | " " " 3 |
| P5 23 | CPU 3* | " " | P5 33 | CDO 4* | " " " 4 |
| P5 24 | CPU 4* | " " | P5 34 | CDO 5* | " " " 5 |
| P5 25 | CPU 5* | " " | P5 35 | CDO 6* | " " " 6 |
| P5 26 | CPU 6* | " " | P5 36 | CDO 7* | " " " 7 |
| P5 27 | CPU 7* | " " | P5 37-40 | GRD | Signal Ground |

### 3.2.3 P8 Power, Write Protect, Miscellaneous

| PIN# | SIGNAL NAME | DESCRIPTION |
|---|---|---|
| P8 1 | WP3* | Ground to Write Protect Unit 3 |
| P8 2 | WP1* | Ground to Write Protect Unit 1 |
| Key | | |
| P8 3 | LDRFAL | LED Driver indicates Drive Fail Status |
| P8 4 | LCRC | LED Driver indicates CRC Error |
| P8 5 | LUN 1 | LED Driver indicates Unit Select Bit 1 = 1 |
| P8 6,7,8,9 | +5 V | +5 V input |
| P8 10 | -12 V | -12 V input |
| P8 A | WP2* | Ground to Write Protect Unit 2 |
| P8 B | WPØ* | Ground to Write Protect Unit Ø |
| P8 C | L BUSY | LED Driver indicates Unit Busy |
| P8 D | LWRPR | LED Driver indicates Unit Write Protected |
| P8 E | LUN Ø | LED Driver indicates Unit Select Bit Ø = 1 |
| P8 F,H,J,K,L | GRD | Ground return for +5V and -12V |

## IV. POWER REQUIREMENTS

4.1 CF360 +5VDC, ± 5% @ 6 Amps
-12VDC, ± 5% @ 1 Amp

4.2 Disk Drive - The CF360 is ideally suited for use with the Pertec FD400 drive. The FD400 requires +24V ±5% @ 2 Amps Avg, 4 Amps Peak.

## V. COMMAND AND DATA STRUCTURE

5.1 Commands and Command Word Bits

| COMMAND | CPU BIT (NEGATIVE TRUE) | | | | | | | | HEX CODE |
|---|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Examine Status | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| Read | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 03 |
| Write | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 05 |
| Read CRC | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 07 |
| Seek | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 09 |
| Clear Error Flags | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0B |
| Seek Track Ø | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0D |
| Write with DDAM* | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0F |
| Load Track Address | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11 |
| Load Unit/Sector | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21 |
| Load Write Buffer | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 31 |
| Shift Read Buffer | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 41 |
| Clear | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 81 |
| Examine Read Buffer | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 40 |

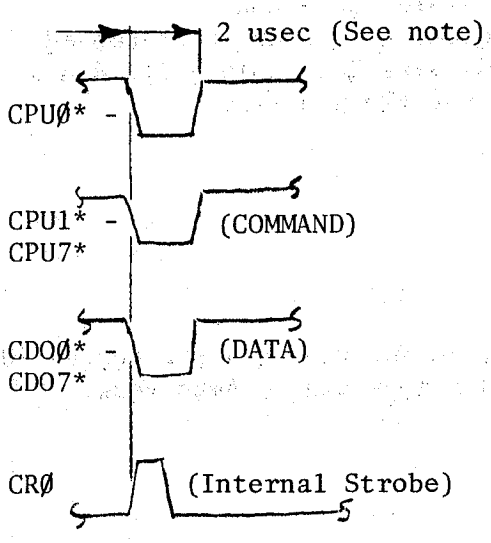
* DDAM = Deleted Data Address Mark

Please refer to Fig. 3 for timing requirements of command and data outputs.

## 5.2 Status/Data Input Lines

| | |
|---|---|
| DIØ | Data In Ø / Busy |
| DI1 | Data In 1 / UN Ø Unit Select Code Bit Ø |
| DI2 | Data In 2 / UN 1 Unit Select Code Bit 1 |
| DI3 | Data In 3 / Media Error or CRC Error |
| DI4 | Data In 4 / Selected Unit Write Protected |
| DI5 | Data In 5 / Drive Fail (not up to speed, etc.) |
| DI6 | Data In 6 / No status Bit (Always Logic 1) |
| DI7 | Data In 7 / Found Deleted Data Address Mark |

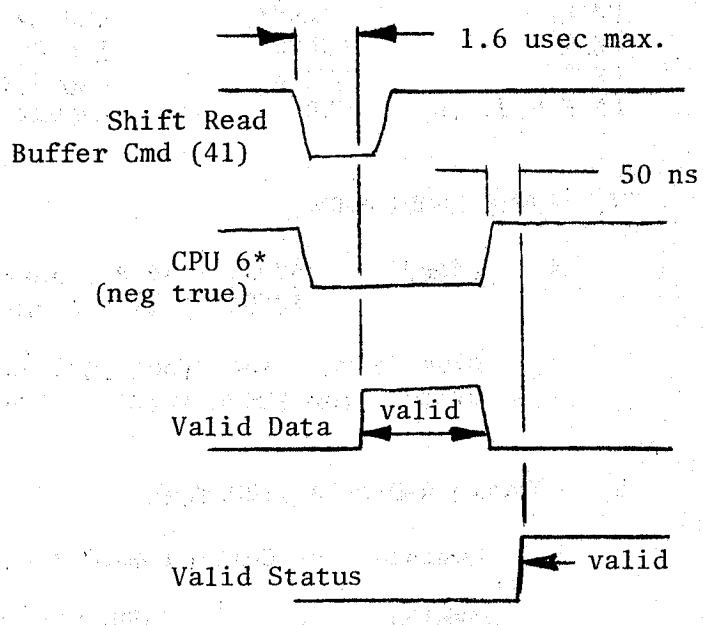
Please refer to Figure 4 for timing of data and status inputs.




NOTE: Other date pulse widths can be accomodated, consult iCOM.

Output Command and Data Timing

Fig. 3




Input Status and Data Timing

Fig. 4

## 5.3 Data Output Lines

| | CDO Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Range |
|---|---|---|---|---|---|---|---|---|---|
| Track Address | Ø MSB | | | | | | | LSB | ØØ to 4C (HEX) |
| Unit/Sector | Unit MSB LSB | Ø | MSB | | Sector | | | LSB | Unit 0-3<br>Sector 1-1A (HEX) |
| Write Buffer | MSB | | | | | | | LSB | ØØ to FF (HEX) |

## 5.4 Operation Sequences

### 5.4.1 Seek

a) Set up Data Out Bits 0-7 with Unit & Sector
b) If track remains same, execute a load Unit/Sector Command (21). Otherwise, set up data out bits with Track Address
c) Execute a load Track Address command (11)
d) Execute a Seek command (09)
e) If interrupt is used floppy will pulse "Done" when operation complete. More typically, the microcomputer should loop-on-busy as follows
f) Execute an Examine Status command
g) Input the data lines and check the busy (=0 when done) and CRC bits.

### 5.4.2 Seek Ø

a) Always used on power up
b) No track address necessary
c) Execute a Seek Ø command (OD)
d) Loop-on-busy as above. Selected unit will go to track Ø.

### 5.4.3 Read

a) After seek to the correct track, unit and sector, execute read (03)
b) Loop-on-busy
c) Check CRC, reread if DI# = 1
d) Execute examine read buffer (40)
e) Input 1st character from data input lines
f) Shift read buffer (41)
g) Repeat (f) & (g) until 128 characters have been read.

### 5.4.4 Write

a) Load write buffer by first setting up Data Out lines
b) Execute Load Write Buffer (31)
c) Repeat (a) and (b) above until 128 characters have been loaded
d) Seek to correct track, unit, & sector
e) Execute write (05)
f) Execute read (CRC) (07) (Does not alter contents of read buffers) See also 6.1.2.
g) Check CRC Bit and repeat (e) and (f) if CRC = 1. Write Buffer recirculates so it is not necessary to reload it to rewrite.

### 5.4.5 Write with Deleted Data Address Mark

a) Same as write except that the data when written is automatically preceded by a Deleted Data Address Mark (DDAM) instead of by the standard Address Mark. When the same sector is later read, the Found Deleted Data Address Mark Status bit will be set on completion. This command can therefore be used to identify the data for some purpose. For example, a DDAM can be used to indicate the end of a long data field. It could also be used in some editing function.

5.4.6 Clear Error Flags

a) Used to clear Deleted Data Address Mark and cyclic Reduncdancy Check status bits.
c) Execute Clear Error Flags command (OB)

5.4.7 Clear

a) Execute Clear command (81)
b) Halts any operation in process. Clears Busy and pulses Done.

5.5 Status

5.5.1 7 Status Bits are returned on the Data Input Lines, DIØ thru DI 7, when command Bit 6, CPU 6*, is logic Ø. All bits are negative true.

5.5.2 Busy. When logic "1", indicates that an operation is in process. When logic "0", indicates operation done. Busy is also cleared by Clear, Clear Error Flags, or the head unloading.

5.5.3 UNØ, UN1 Unit Select Code Bits:

| UN1 | UNØ |
|---|---|
| 0 | 0 = Unit 0 Selected |
| 0 | 1 = Unit 1 Selected |
| 1 | 0 = Unit 2 Selected |
| 1 | 1 = Unit 3 Selected |

5.5.4 Media Error or CRC Error. Indicates that the Read or Read (CRC) operation resulted in a data error. The status bit should be cleared by a Clear Error Flags command and the data should reread or rewritten.

5.5.5 Selected Unit Write-Protected. Each of the drives can be write-protected manually. If so protected this status bit will equal logic "1" when that unit is selected.

5.5.6 Drive Fail. Indicates that the selected drive is not ready because the door is open, or the drive is not up to speed, or no diskette is installed, or no drive is installed.

5.5.7 Found Deleted Data Address Mark. If on a Read command the data is preceded by a DDAM then this status bit is set. (See 5.4.5). Status bit is reset by the Clear Error Flags command.

## VI. OPERATION SEQUENCES AND TIMING

6.1 Functional Sequences and Characteristics

6.1.1 Seeks - The FD360/CF360 starts a seek operation by reading its present location from the ID field preceding each sector. A comparison is then made with the desired track address and the head is stepped in the correct direction until the head should be at the right track. The track address is read again and if it compares to the desired track the operation is done.

In some formats the track address may not correspond to the physical track number, due to tracks being declared down. The FD/CF360 will handle this format by seeking until the correct track address is found

It should be noted that a seek is necessary only to change tracks. To change sectors only, the Load Unit/Sector command is used.

The seek Track Ø can be used to seek to track Ø without regard to the present track. It does not require a transfer of the Track Address. The Seek Track Ø should be used on power up and restart to initialize the head.

6.1.2 Read - A seek to the correct track is necessary unless the head is on the correct track already. A load Unit/Sector command selects the sector to be read, and the CF360 examines the ID Field preceding each Data Sector to find the correct sector. In a standard IBM format diskette, the sectors start at 1 following the index hole and increment to 26 (1A HEX) just before the index hole.

The CF360 automatically computes the CRC during the read and if an error is found the CRC status bit is set at the end of the read. Data from the sector is shifted into the Read Buffer at a 250 Khz rate. When the Read command is complete the first character of the sector is at the front of the read buffer. An examine Read Buffer command (40) will place the Read Buffer output on the Data Input Lines. A shift Read will shift the Read Buffer and place the Read Buffer output on the Data input lines. 127 shifts are thus required to read the 128 Bytes.

A read CRC does not load the data into the Read Buffer but merely tests CRC. This is commonly used following a Write to insure data integrity. Thus a Write operation can be executed and verified without destroying the Read Buffer. This is important in edit operations and for CPU's with small memory.

6.1.3 Write - A write operation writes the contents of the Write Buffer to the selected Unit/Sector. The location of the head while loading the Write Buffer does not matter. After the Write Buffer is loaded, a seek command will move the head to the desired track. The Write Command then causes the CF360 to begin examining each ID field for the correct sector. A field of 6 bytes of "0"'s will then be written preceding the intended location of the data sector. Next, the Address Mark is written (or DDAM if a Write Deleted Data Address Mark command). Then each byte of the Write Buffer is written out, followed by the CRC (2 Bytes) generated by the CF360. Finally, one byte of all zero's or all one's follows the CRC.

The data written should be read by a READ CRC command to insure the operation was valid.

6.2 Operation Timing

6.2.1 Seek

| | |
|---|---|
| Track to Track | 10 msec |
| Head Load & Settling Time | 40 msec, maximum |
| Maximum Seek Time, 77 tracks | 820 msec |

6.2.2 Read/Write

| | |
|---|---|
| Sector Read/Write Time | 6 msec |
| Average Latency (½ Rev) | 83 msec |
| Minimum Latency | 1 msec |
| Read/Write Buffer Shift Rate: | DC to 500 Khz |

## VII. DATA FORMAT

7.1 The CF360/FD360 used standard IBM 33FD type diskettes such as those used in the IBM 3740 series equipment. It is completely media and format compatible. Type 33FD diskettes can be obtained from a number of sources, including iCOM.

7.2 Format Details (each Diskette)

77 tracks per diskette 00 thru 4C HEX
26 Sectors per track 01 thru 1A HEX
128 Bytes (8 Bits) per sector
256,256 Bytes Diskette
1,025,024 Bytes Per FD360 or CF360 using 4 drives.

## VIII. TYPICAL MICROPROCESSOR INTERFACE SCHEMATICS

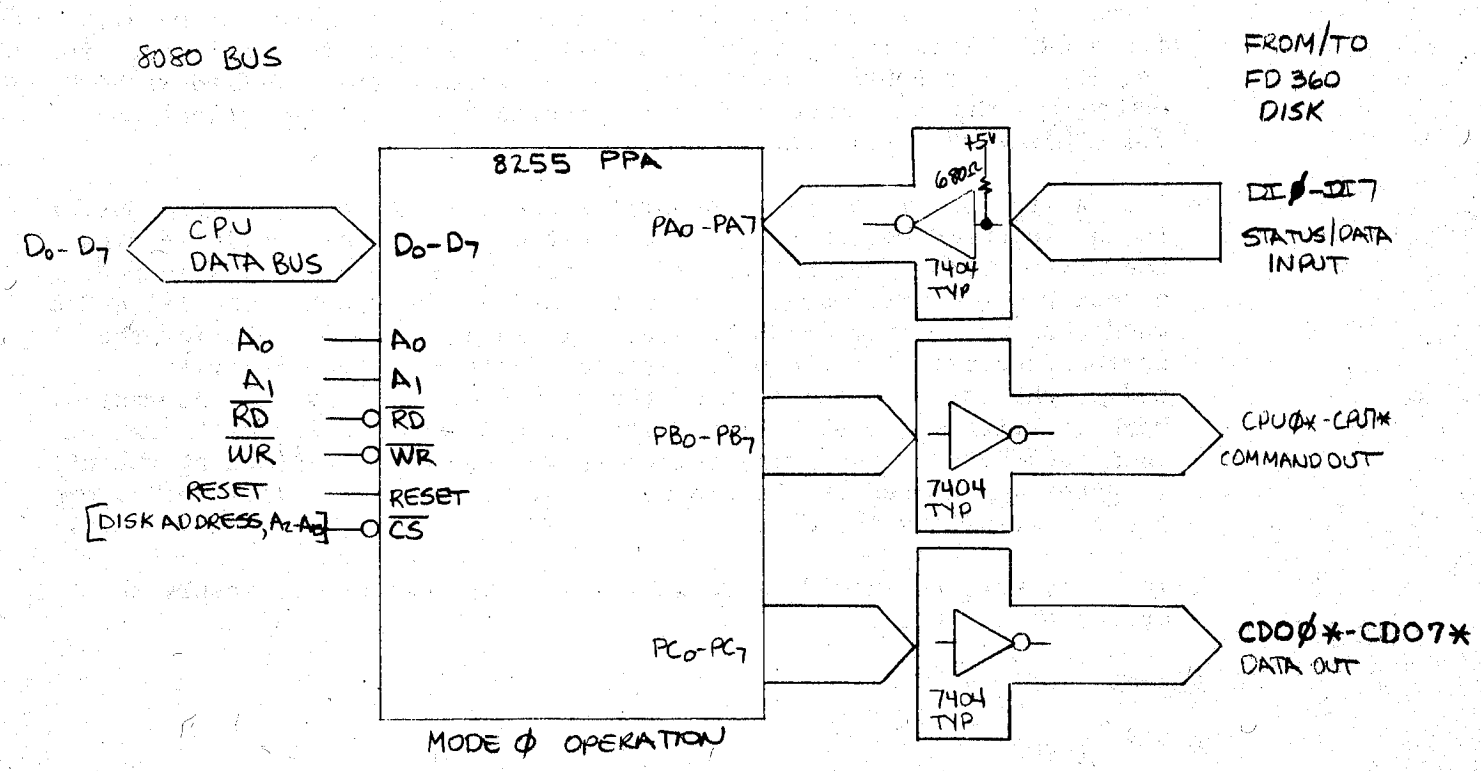



Fig. A-8080 Interface Schematic

VIII. CON'T

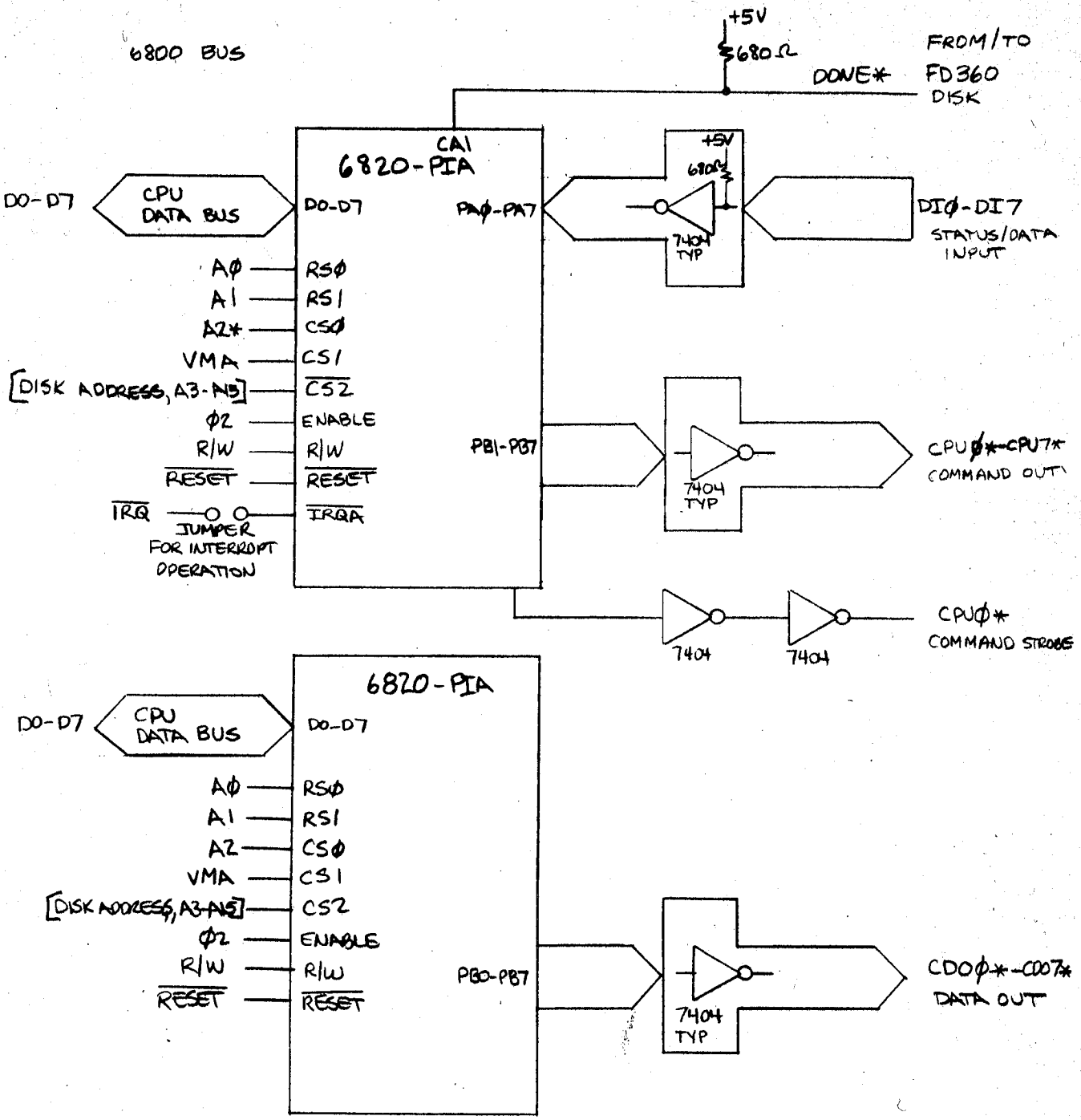



Fig. B-6800 Interface Schematic